CLAIMS

1. A method of operating a power supply controller comprising:

organizing output drive pulses of the power supply controller to into a plurality of sets with each set of the plurality of sets having a plurality of timing slots for the output drive pulses;

deleting a first drive pulse in a first set of the plurality of sets from a first timing slot when a load current of the power supply controller is less than a first current value; and

deleting the first drive pulse from the first timing slot and a second drive pulse from a second timing slot in a second set of the plurality of sets after the power supply controller has issued the first set.

2. The method of claim 1 wherein deleting the first drive pulse from the first timing slot and the second drive pulse from the second timing slot includes keeping an error voltage of the power supply controller constant.

3. The method of claim 1 wherein deleting the first drive pulse from the first timing slot and the second drive pulse from the second timing slot includes deleting the first drive pulse from the first timing slot and deleting the second drive pulse from the second timing slot that is non-adjacent to the first timing slot.

4. The method of claim 1 wherein organizing the output drive pulses into the plurality of sets with each set of the plurality of sets having the plurality of timing slots includes forming each set with a same number of timing slots.

5. The method of claim 1 wherein organizing the output drive pulses into the plurality of sets with each set of the plurality of sets having the plurality of timing slots includes forming each set with a different number of timing slots.

6. The method of claim 1 further including re-inserting one deleted drive pulse when an output voltage formed by the output drive pulses decreases to a first voltage.

7. A method of forming a power supply controller comprising:

forming the power supply controller to organize output drive pulses into a plurality of sets with each set having a plurality of timing slots for the output drive pulses;

forming the power supply controller to delete a first drive pulse in a first set of the plurality of sets from a first timing slot when a load current of the power supply controller is less than a first current value; and

forming the power supply controller to delete a second drive pulse from a second timing slot in a second set of the plurality of sets after the power supply controller has issued the first set.

8. The method of claim 7 wherein forming the controller to delete the second drive pulse from the second timing slot includes forming the controller to delete the first drive pulse from the first timing slot and the second drive pulse from the second timing slot.

9. The method of claim 8 wherein forming the controller to delete the first drive pulse from the first timing slot and the second drive pulse from the second timing slot includes forming the controller to delete the first drive pulse from the first timing slot and the second drive pulse from the second timing slot that is non-adjacent to the first timing slot.

10. The method of claim 7 wherein forming the controller to organize the output drive pulses into the plurality of sets with each set having the plurality of timing slots includes forming the controller to form each set with sixteen timing slots.

11. The method of claim 7 wherein forming the controller to organize the output drive pulses into the plurality of sets with each set having the plurality of timing slots includes forming the controller to form each set with a different number of timing slots.

12. The method of claim 7 further including forming the controller to re-insert at least one deleted drive pulse when an output voltage formed by the output drive pulses decreases to a first voltage.

13. The method of claim 7 further including forming the controller to delete all drive pulses from a set.

14. The method of claim 12 further including forming the controller to re-insert all deleted drive pulse when an output voltage formed by the output drive pulses decreases to a second voltage that is less than the first voltage.

15. The method of claim 7 further including forming the controller to maintain an error voltage constant during each set of the plurality of sets.

16. The method of claim 7 wherein forming the controller to delete the first drive pulse in the first set of the plurality of sets from the first timing slot when the load current of the power supply controller is less than the first current value includes counting a first number of current reversals through an energy storage inductor to determine when the load current of the power supply controller is less than the first current value.

17. A power supply controller comprising:

an output coupled to drive an output transistor to provide a load current through an energy storage inductor to form an output voltage; and

a control block coupled to organize drive pulses to the output transistor into a plurality of sets having a plurality of timing slots for driving the output transistor wherein the control block provides a control signal to delete a first drive pulse in a first set of the plurality of sets from a first timing slot when the load current is less than a first current value.

18. The power supply controller of claim 17 wherein the control block coupled to organize drive pulses includes the power supply controller providing the control signal to delete a second drive pulse from a second timing slot in a second set of the plurality of sets after the power supply controller has issued the first set.

19. The power supply controller of claim 17 wherein the control block coupled to organize drive pulses includes the power supply controller coupled to re-insert at least one deleted drive pulse when the output voltage decreases to a first voltage.

20. The power supply controller of claim 19 wherein the control block coupled to organize drive pulses includes the power supply controller coupled to re-insert all deleted drive pulse when the output voltage decreases to a second voltage that is less than the first voltage.